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Final Design and Integration of Micro-Chip Inductive Edge Sensors for the Seven Segment Demonstrator

**Final Report for Testing of Integrated Edge Sensors in
Test Packages**

15 April 1997

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Prepared By:
Mr. John Karpinsky
SY Technology, Inc.

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by John Karpinsky
SY Technology, Inc.
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We have tested both the devices that we had packaged by MOSIS and those packaged by GTRI. The testing of the MOSIS parts was incomplete because there was some internal damage to that device and the earlier tests that were done on that device were not repeatable later in the testing. The things that were established in the early testing was as follows.

- 1) The input amplifier for the 10 MHz signal functions, although it did not have as large an amplitude as was expected at 10 MHz.
- 2) The comparators function well but the speed was not measured on this first device.
- 3) The exclusive OR also functions well and has ample speed to provide the phase information to the filters.
- 4) The filters also function well but there is a problem with noise from the power lines coupling into the filtered signal.
- 5) Then, during testing, the amplifier stopped functioning, and it was not possible to continue testing.

Figure 1 shows the integrated circuit layout with the location for the coils indicated by the spiral shapes on the layout. The bonding pads are at the bottom of the device.

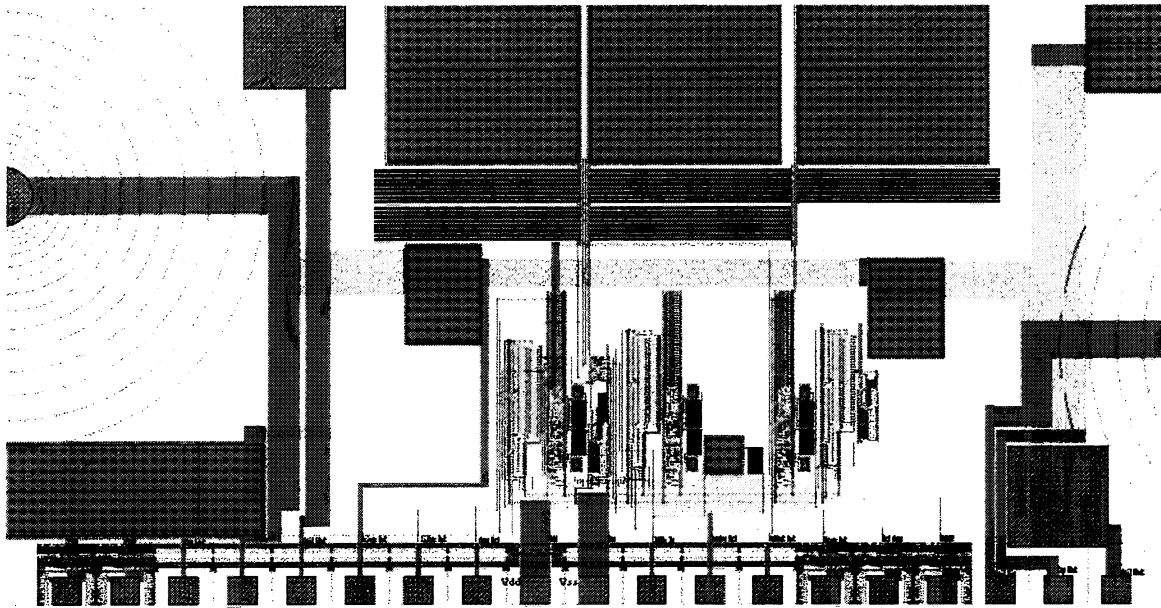


Figure 1, Integrated circuit layout showing bonding pads and circuitry

Because there was only one part that was packaged, we were not sure whether the problems with the part were due to a design problem or due to a defect in that one packaged part. Therefore, John Karpinsky of SY Technology and Bill Robinson of GTRI put some unpackaged parts on a probe station at Georgia Tech. The result of this testing was that by themselves, each section of the circuit functioned. It was not possible to test to whole circuit at once because of the limited number of pads that could be probed at once. However, this was a promising result.

At that point, we decided to package some more parts, and GTRI was asked to do that. John Karpinsky sent them some unpackaged chips and they wire bonded two more devices. Then, these devices were tested further at SY Technology. The results of this testing were as follows.

- 1) The input amplifier output for the 10 MHz input was still lower than expected. The signal amplitude at lower frequencies was much better which indicates that the bandwidth of the amplifier was less than anticipated. This was probably because in an attempt to reduce that power consumption of the device, the current flow was reduced too much and thus the slew rate and the small signal bandwidth were both compromised. In addition, when the coils were connected to the chip, the amplitude was reduced even further and the signal was not sufficient to drive the coils. In addition, the amplifier output is modulated by the exclusive OR signals. This completely destroys the 10 MHz signal going to the coils and comparators. This is because the same power buses are sending the power to the exclusive OR circuits as to the bias generator for the amplifier as is shown in figure 2. The exclusive OR circuits are at the right of the figure with the arrow pointing at them. The large circuit in the middle is the bias generator, and the small circuit on the left is the bias splitter. The power busses are the wider blue horizontal lines on the top and bottom of the circuits. This power bus fluctuation is modulating the bias to the amplifier when the exclusive OR circuits switch. That bias is a very important voltage for the amplifier as it controls the current supplied to the input sensing transistors. This current is being disturbed when the digital circuits switch.
- 2) The comparator switching time delay is about 30 nano seconds(ns) out of the 100 ns cycle time at 10 MHz. This is sufficient but marginal because it limits the measurable phase delay to about 125 degrees instead of 180 degrees.
- 3) The exclusive OR circuit switches very fast and with only a couple of ns of delay.
- 4) The filters which convert the digital pulse width modulated signal into a DC voltage function well, but there is noise on the signal lines which is coupled from the exclusive OR and comparator switching transients.
- 5) It has been found to be very difficult to mount the coils directly on the chip as was originally planned. We are now trying to leave them on the silicon substrate that they were fabricated on and connecting them to the edge sensor driver and sensing circuitry with flexible cable.

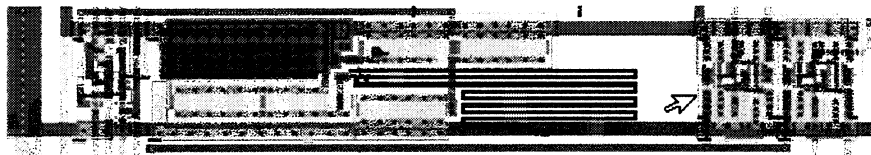


Figure 2, Exclusive OR and bias generator on the same power bus

Therefore, here are our recommendations for the next phase of the edge sensor development. We will redesign the chip to correct the deficiencies noted above. Specifically, the following changes will be incorporated in the new edge sensor system design.

- 1) First, the chip will be packaged in a conventional 16 pin DIP package to minimize the packaging costs. This will limit the number of test points that can be monitored from the packaged part. This should not be a problem because we already know that the comparator and exclusive OR circuits work, and we do not need to monitor the internal functioning of the filter. Only the final output is important in any case.
- 2) In addition, two additional power pins will be added to enable separating the digital power from the analog power. This will help both the bias generators and the filters which need very low noise power.

- 3) The amplifier will be redesigned to improve the driving current capability to drive the coils and increase the slew rate and band width. The original amplifier implemented in the Phase 1 SBIR worked just fine, but when we redesigned the amplifier for less power consumption, we went too far. We will re-evaluate the power/ drive current trade off and design an optimized circuit.
- 4) The comparator will be redesigned as well to decrease the switching delay time. This was another circuit that was starved for current to decrease the power consumption. Again, the power speed trade off will be re-evaluated.
- 5) All of the power busses and biases will be carefully laid out to reduce the coupling of the high frequency signals with the biases and filter output. In addition, on chip decoupling capacitors will put where ever possible. After the circuit components are placed, the empty spaces on the chip will be filled with decoupling capacitors
- 6) The external coils will be redesigned for easy connection to the integrated circuit, and low cost fabrication.

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13. ABSTRACT (Maximum 200 words) The contractor attended the critical design review and evaluated the presentations of other team members and presented data on the inductive edge sensor. The prototype micro-chip inductive edge sensor was evaluated, and devices were found to have a number of characteristics which made them unsuitable for installation on the seven segment demonstrator. The amplifier bandwidth was too low, the output drive current was too small, and there is an interaction between the digital circuitry and the amplifier that causes the amplifier to stop functioning. Therefore, the inductive edge sensors were not installed on the seven segment demonstrator. The contractor has participated in instruction, problem analysis, and provided technical assistance to NASA and its contractors for the development of 8 hexagonal mirror faceplates with electronics and edge sensors.				
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